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(54) Integrated semiconductor circuit including protection means.

(57) The invention relates to a circuit which is integrated on a semiconductor substrate in order to drive a load, (for example, a VFD) by means of a comparatively high voltage (for example, 35 V), comprising a first and a second supply voltage terminal for application of the comparatively high voltage, an input, and a load output whereto a load to be driven by the circuit can be connected, there also being provided a switching transistor, a protection transistor and a sub-circuit, the switching transistor and the protection transistor being connected in series, the gate of the switching transistor being connected to the input, the source of the switching transistor being connected to a first supply voltage terminal, and the drain of the protection transistor supplying a signal for the sub-circuit during operation, the output of the sub-circuit being connected to the load output and the gate of the protection transistor receiving a fixed voltage, the protection transistor being conceived so that it limits the voltage at the drain of the switching transistor.

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The invention relates to a circuit which is integrated on a semiconductor substrate for level conversion or for driving a load (for example, VFD = Vacuum Fluorescence Displays) with a comparatively high voltage (for example, 35 V), comprising a first and a second supply voltage terminal for application of the comparatively high voltage, an input and an output, there also being provided a switching transistor, a protection transistor and a sub-circuit, the switching transistor and the protection transistor being connected in series, the gate of the switching transistor being connected to the input, the source of the switching transistor being connected to a first supply voltage terminal, and the drain of the protection transistor supplying a signal for the sub-circuit during operation, an output of the sub-circuit being connected to the output and the gate of the protection transistor receiving a fixed voltage.

A circuit of this kind is known from Proceedings of the IEEE Custom Integrated Circuits Conference, Portland, Oregon, May 4-7, 1987, pp. 267-271. In circuits of this kind it is important to ensure that no breakdowns occur in any location due to excessive field strengths especially at the drain or gate junctions.

It is an object of the invention to propose a circuit integrated on a semiconductor substrate in which the vulnerability of the circuit to the comparatively high voltage for driving the load connected to the circuit is substantially reduced or even eliminated, without additional technology and without complex process steps being used.

To achieve this, an integrated circuit on a semiconductor substrate in accordance with the invention is characterized in that the protection transistor is conceived so that it limits the voltage at the drain of the switching transistor.

An embodiment of the integrated circuit in accordance with the invention is characterized in that the gate of the protection transistor is provided on the field oxide layer of the integrated circuit. Because the gate of the protection transistor is provided on the field-oxide layer of the integrated circuit in accordance with the invention, the threshold voltage of such a transistor is much higher (for example, 26 V) than in conventional transistors; this is due to the thickness of the field oxide. The so-called "body effect" also makes a contribution in this respect. The threshold voltage V_{TX} of a MOSFET can be expressed as:

$$V_{TX} = V_{TO} - \gamma \left[\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right]$$

for p-channel MOS transistors (for n-channel transistors, $-V_{BS}$ and γ should be inserted in this equation),
where:

V_{TO}: threshold voltage for $V_{BS} = 0$
V_{BS}: bulk-source voltage
ϕ_F: Fermi potential: $(kT/q) \ln(N/Ni)$
and

$$\gamma = \frac{\sqrt{2\varepsilon_s q N_D}}{C_{ox}}$$

Therein,
ϵ_s: dielectric constant of silicon
N_D: density of the charge carriers in bulk (donators for p-channel MOS transistors, acceptors for n-channel MOS transistors)
N: surface concentration in channel region
N_i: intrinsic concentration of the charge carriers in the purified material sample
q: elementary charge
and
C_{ox}: ϵ_{ox}/t_{ox}
where
ϵ_{ox}: dielectric constant of the oxide layer
t_{ox}: thickness of the oxide layer.

Conventional MOS transistors have a comparatively thin oxide layer (= 30-50 nm) between the gate and the channel region. Because the gate of the protection transistor is provided on the thick field oxide (thickness 0.8-1 µm) already present in any integrated circuit, a comparatively high threshold voltage is obtained. For V_{TO} a parasitic threshold voltage (dielectric in the form of field oxide instead of gate oxide) of from approximately 12 to 15 V is concerned. Added thereto is a strong body effect, because γ is inversely proportional to C_{ox} which is small because of t_{ox}. This high threshold voltage prevents the occurrence of a breakdown at the drain diode of the switching transistor during operation, because the potential at the drain of the switching transistor remains limited. The protection transistor is turned off already before the drain potential of the switching transistor has dropped so far that a breakdown of the cited diode occurs.

A further embodiment of the integrated circuit in accordance with the invention is characterized in that the switching transistor comprises an extended drain and/or the protection transistor comprises an extended drain and an extended source. An extended drain or source region is formed when the well material is used to envelop the p^+ in a p-channel transistor in p-well technology or the n^+ in an n-channel transistor in n-well technology. The breakdown strength of the drain or source region is thus increased.

A further embodiment of the integrated circuit in accordance with the invention is characterized in that the sub-circuit comprises a resistance. The

switching transistor, the protection transistor and the resistance together form a level converter having an output terminal connected to the drain of the protection transistor

A further embodiment of the integrated circuit in accordance with the invention is characterized in that the sub-circuit comprises a current-amplifier circuit which is conceived as an emitter-follower circuit comprising two vertical integrated bipolar transistors forming a Darlington pair. The sub-circuit serves for impedance conversion. In the case of an n-substrate, a Darlington pair is appropriate in this respect, because the logic high state must be low-ohmic for VFD drivers.

A further embodiment of the integrated circuit in accordance with the invention is characterized in that the sub-circuit comprises a further switching transistor whose source is connected to the second supply voltage terminal, whose gate is connected to the drain of the protection transistor, and whose drain is connected to the first one of a series-connected cascode of further protection transistors, the drain of the last further protection transistor of the cascode being connected to the output, the gates of the cascode of further protection transistors being connected *via* a series connection of resistances, the output being connected to the emitter of a switch-off transistor whose collector is connected to the first supply voltage terminal and whose base is connected, *via* a resistance, to its emitter and to the drain of a further transistor whose source is connected to the first supply voltage terminal and whose gate is connected to the drain of the protection transistor, the cascode of resistances being proportioned so that the voltages at the drain-gate junctions and at the drain-source junctions of the further switching transistor and the further protection transistors are limited. In VFD drivers, the logic high state should be low-ohmic. In the case of a p-substrate, a Darlington pair cannot be used for this purpose, because the dual switching element is a pnp substrate transistor which can make only the logic low state low-ohmic. Therefore, in accordance with the invention the cascode of the further switching transistor and the further protection transistors is used to make the high state low-ohmic. The gate voltage of the protection transistors is comparatively low in the switched-on state. In the switched-off state the voltages are separated so that each transistor has to cope with only a part of the overall load.

A further embodiment of the integrated circuit in accordance with the invention is characterized in that the gate of the protection transistor is connected to the second supply voltage terminal. This embodiment is advantageous because no further fixed voltage of a value between the voltage levels of the two supply voltage terminals need be provided for the gate of the protection transistor.

The invention will be described in detail hereinafter with reference to embodiments shown in a drawing; therein:

Figs. 1A, B, C and D show a preferred embodiment of a circuit in accordance with the invention;

Figs 2A and B show an embodiment of a further circuit in accordance with the invention;

Fig. 3 shows a further embodiment of a circuit in accordance with the invention, and

Fig. 4 shows an embodiment of a circuit in accordance with the invention which can be integrated on a p-substrate.

Fig. 1A shows a preferred embodiment of a circuit in accordance with the invention. The circuit is used, for example for driving vacuum fluorescence displays. A supply voltage of 5 V and -30 V is then applied to the supply voltage terminals VDD and VEE, respectively. The circuit comprises a first PMOS switching transistor T1, a second PMOS, protection transistor T2, a sub-circuit comprising two bipolar npn transistors T3 and T4 which form a Darlington output stage, and three resistors R1, R2 and R3. The PMOS transistor T1 is a conventional transistor having a drain D1 and a source S1 which are constructed as p^+ regions D1, S1 (see Fig. 1B) in a substrate of n-material, the gate oxide having a thickness of from 30 to 50 nm. The gate G1 receives an input signal Vin. The input signal Vin has, for example two logic levels: VDD (= 5 V)and VSS(=0 V).

The protection transistor T2 (see Fig. 1C) has a p^- drain D2p^- and a p^- source S2p^- which are connected *via* p^+ regions. The polysilicon gate G2 is arranged on the field oxide FO1. Consequently, as has already been explained, the transistor T2 has a threshold value (for example, $V_{T2} \approx$ -28 V for $V_{BS} \approx$ 2.5 V; $V_{T2} \approx$ -35 V for $V_{BS} \approx$ 5 V) substantially higher than that of the switching transistor T1 ($V_{T1} \approx$ 1 V). The drain D2p^- and the source S2p^- are connected *via* A1 contacts provided in the insulating silicon oxide layer SO1.

The bipolar transistors T3 and T4 are constructed as vertical integrated transistors as appears from Fig. 1D. In the substrate SB of n^- material, provided on the n^{+*} semiconductor substrate material as an epitaxial layer, there is formed a p^- tub W. In said tub W there are formed a p^+ region as the base B3 and an n^+ region as the emitter E3,the collector C3 of the bipolar transistors T3 and T4 being connected to the supply voltage VDD *via* an n^+ region in the substrate SB. The use of n^{++} substrate material renders the circuit less sensitive to latch-up problems. Moreover, the collector supply lead resistance is reduced, which is particularly advantageous for a Darlington output stage. The resistances R1 (10 kΩ), R2(10kΩ) and

R3 (100 kΩ) can be formed as a respective p^- tub in the n^- layer. The resistance R3 need not be integrated. It can be connected, outside the integrated circuit between the load output O1 and the supply voltage VEE.

The circuit in accordance with the invention as shown in Fig. 1 operates as follows. When an input voltage VSS (= 0 V) is applied to the input terminal Vin, the transistor T1 is turned on. The transistor T2 is also turned on, because the gate G2 is maintained at the fixed voltage VEE (= -30 V), so that the base of the transistor T3 becomes substantially equal to V_{DD}. The output voltage Vout is raised *via* the Darlington pair T3 and T4 (Vout ≈ VDD -2. V_{BE}; V_{BE} = base-emitter voltage of the transistors T3 and T4). The Darlington pair T3, T4 ensures suitable drive power at the load output O1.

When the input voltage Vin is changed from 0 V to V_{DD}, the transistor T1 is turned off. As a result, the transistor T2 can no longer supply current. Consequently, the base of the transistor T3 drops to V_{EE}. The voltage at the source S2 of the protection transistor T2 also drops towards V_{EE}. When the voltage difference between the gate and the source of the second transistor T2 drops below the threshold voltage V_{TK} (≈ -26 V), the protection transistor T2 is turned off. Consequently, the potential at S2 remains limited to voltages in the vicinity of V_{DD}. The transistor T2 is turned off before its source drops below V_{SS}, because (as stated) the threshold voltage V_{T2} ≈ -35 V for V_{BS} = 5V. The transistor T1 is thus protected against drain and gate/drain breakdowns.

Fig. 2A shows a further embodiment of a circuit in accordance with the invention in which the sub-circuit (comprising transistors Q21, Q22 and resistances R21, R22 and R23) can be identical to the corresponding sub-circuit (comprising transistors T3, T4 and resistances R1, R2 and R3) of Fig. 1A and can also have the same function: impedance conversion for a load to be connected to the load output O2 (Fig. 2A), for example a vacuum fluorescence display. The transistors Q21 and Q22 are vertical npn transistors and the resistances R21, R22 and R23 may be P-well resistances. It is not absolutely necessary to integrate also the resistance R23. It can also be connected, outside the integrated circuit, between the load output O2 and the supply voltage V_{EE}.

Two transistors, *i.e.* a switching transistor P21 and a protection transistor P22, are connected in series between the supply voltage V_{DD} and the sub-circuit comprising the transistors Q21, Q22 and the resistances R21, R22 and R23.

The control voltage V_{in} varies between V_{DD} and V_{SS}. It is applied to the gate G21 of the transistor P21. The PMOS transistor P21 is a conventional MOS transistor, except for the construction of its drain. The drain DP21 is an "extended" drain which is thus capable of withstanding higher voltages, without a breakdown occuring at the drain. An extended drain or source region is formed by using the tub material to envelop the p^+ in a p-channel transistor in p-tub technology or the n^+ in an n-channel transistor in n-tub technology. Thus, a higher breakdown strength of the drain or source region is obtained in the "extended" version relative to the substrate material. The protection transistor P22 comprises a gate G22 which is connected to a fixed voltage V_M; for example, $V_M = (V_{DD} + V_{EE})/2$ in the example of Fig. 2. The extended drain and the extended source are special aspects of this transistor. Fig. 2B is a diagrammatic cross-sectional view of the transistor P22 (not to scale). In the substrate L of n^- semiconductor material there are provided two tubs WD and WS of p^- semiconductor material, which tubs constitute the drain and the source of the transistor P22. The source and drain connections consist of p^+ material. They are surrounded by the thick field oxide FO2. The gate GP22, being insulated from the n^- substrate L by a gate oxide layer, extends between the source and the drain and may overlap the thick field oxide layer FO2. The paths dD and dS between the field oxide FO2 and the n^- material are sufficiently large to make misalignment between gate and drain/source regions acceptable.

The operation of the circuit shown in Fig. 2A is as follows: when a potential V_{SS} (= 0 V) is applied to the gate G21 of the transistor P21, the transistor P21 is turned on and hence also the transistor P22, because the source potential approaches V_{DD} (= + 5 V). The voltage between the gate G22 and the source S22 amounts to approximately -17.5 V. The current flowing through the transistors P21 and P22 will turn on the Darlington transistor pair Q21 and Q22, thus driving a load connected to the load output O2.

As soon as the voltage V_{in} at the gate G21 increases and reaches $V_{DD} - |V_{TH}|$, the transistor P21 is turned off. The voltage at the drain D21 then decreases until the gate-source voltage of the transistor P22 decreases to V_{TH} (the source voltage is then slightly lower than the fixed voltage $V_M + 1V_{TH}$). The drain voltage for the transistor P21 is thus limited to the range from ≥ V_{DD} - 17.5 + | VTH | = -11.5 V which can be withstood by an extended drain construction. The drain-gate voltage for the transistor P22 also remains below -20 V ($V_{EE} - V_M$ ≈ -17.5 V). The operation of the transistor P22, therefore, is not endangered by a drain-gate breakdown.

Fig. 3 shows a further embodiment of a circuit 30 in accordance with the invention. The circuit 30 comprises a switching transistor P31 and two protection transistors P32 and P33. These transistors

are connected to one another and to a sub-circuit (consisting of transistors Q31, Q32 as well as resistors R31, R32 and R33), in series between the supply voltage V_{DD} (+5 V) and the load output O3. The circuit 30 can be integrated on a semiconductor substrate, the load output O3 being connected to an output terminal of the integrated circuit, for example in order to drive a vacuum-fluorescence display.

The components Q31, Q32, R31 and R32 of the sub-circuit are identical or similar to the components T3, T4, R1 and R2 and have the same function. It is not absolutely necessary to integrate also the resistor R33. It can be connected, outside the integrated circuit, between the load output O3 and the supply voltage V_{EE}. The transistor P31 is a conventional MOSFET having a gate oxide layer of normal thickness (30-50 nm). Except for the extended drain (see Fig. 2B), the transistor P32 is also a conventional transistor, as is the transistor P31. The transistor P33 is a parasitic transistor whose gate GP33 is provided on the (thick) field oxide (see Fig. 1C). The gate GP33 of the transistor P33 carries a fixed potential V_{EE} (≈ -30 V). The gate GP32 of the transistor P32 carries a fixed potential V_C ($V_C = V_{DD} - \frac{1}{2}(V_{DD}-V_{EE}) \approx -4V$). The gate GP31 of the switching transistor P31 receives the control voltage V_{in} ($0 \leq V_{in} \leq 5V$). When the control voltage equals 0 V, the transistors P31, P32 and P33 are turned on and apply current to the transistors Q31 and Q32. A load connected to the load output O3 is thus driven.

When the control voltage V_{in} increases to 5 V, the transistor P31 is turned off. The voltage at the drain DP31 decreases to $V_C + |1V_{TH}|$, so to ≈ -3 V. The potential difference between the drain DP31 and the gate GP31 or the substrate amounts to approximately 8 V; this is far less than would be required for a breakdown.

The voltage at the drain DP32 itself decreases until the transistor P33 is turned off. This occurs when $V_{EE} + |V_{TP}|$ is reached, where V_{TP} is the parasitic threshold voltage. The voltage difference between the extended drain DP32 and the gate GP32 should not exceed 15 V. In other words, for a gate voltage of $V_C \approx -4$ V, the voltage at the drain DP32 may not drop below -19 V. The threshold voltage $|V_{TP}|$ of the transistor P33 should amount to ≥ 11 V; this is generally the case.

Fig. 4 shows a further embodiment of a circuit 40 in accordance with the invention which can be integrated on a p-substrate. This circuit 40 comprises an NMOS switching transistor MN1, an NMOS protection transistor MN2, and a sub-circuit which is connected in series between two supply voltages V_{PP} (≈ + 30 V) and V_{SS} (= 0 V). The sub-circuit comprises resistances R41, R42, R43, bipolar pnp transistors Q41 and Q42, a (parasitic) NMOS transistor MN3, further resistances R44, R45, R46, R47 and R48, and PMOS transistors MP1, MP2, MP3, MP4 and MP5. Fig. 4 also shows the load to be powered by the circuit 40. It concerns a capacitance CL with parallel-connected resistance RL connected to the load output O4.

The resistances R41 to R43 are connected to one another and in series with the transistors MN1 and MN2 between V_{PP} and V_{SS}. The transistors MP1, MP2, MP3, MP4 and Q41 are connected in series between V_{PP} and V_{SS}, the collector of the transistor Q41 being connected to V_{SS} and its emitter to the drain of the transistor MP4. The sources of MP4, MP3, MP2 and MP1 are connected to a respective drain of the transistors MP3, MP2, MP1 and to V_{PP}. The gate GMP1 of the transistor MP1 is connected to the junction of the resistances R41 and R42. The gate GMP2 of the transistor MP2 is connected to the junction point of the resistances R44 and R45 whereto the emitter of the transistor Q42 is also connected. The collector of the transistor Q42 is connected to V_{SS}, its base being connected to the junction point of the resistances R42 and R43. The gates GMP3 and GMP4 of the transistors MP3 and MP4 are connected to the junction points of the resistances R45 and R46 and of R46 and R47, respectively. The source SMP5 of the transistor MP5 is connected to the resistance R47. The gate GMP5 and the drain DMP5 are connected to one another, to the emitter of the transistor Q41 and to the output terminal O4. Furthermore, the drain DMP5 is connected to the base BQ41 *via* the resistance R48. The drain DMN2 is connected to the gate GMN3 of the transistor MN3 whose source is connected to V_{SS} and whose drain DMN3 is connected to the base BQ41 of the transistor Q41.

In Fig. 4 a plurality of level converters are used to realize a 35 V VFD driver stage on a p substrate. The first level converter consists of MN1/MN2 plus resistances. The circuit still requires the inverted high voltage. This could be generated by inversion of the logic signal by means of the subsequent second level converter. However, it is simpler to achieve the inversion at the high voltage side by directly driving the "protection transistor". The inverter and the switching transistor can then be dispensed with. This results in the structure consisting of MN3 with the resistances R44-R48. Finally, MP1 may be considered to be a switching transistor in the context of the invention. The associated protection structure is the cascode with MP2-MP4. Instead of Q41, use could be made of a resistance (however, because of the faster switch-off, the active load Q41 offers advantages for practical applications of the VDF driver).

Q41 could be driven by a separate level converter (of the same polarity as MN3/rosistances). That, however, would increase the complexity.

Therefore, dual use is made of the level converter MN3/resistances. The use of the same level converter for two purposes (driving Q41 and bias for the cascodes MP2-MP4) gives rise to a conflict at output O4 on VPP. MP5, connected as a diode, serves for decoupling.

Finally, the two level converters MN1/MN2/resistances and MN3/resistances are coupled via Q42. Q42 may be considered to be a "sub-circuit" (connected this time as an emitter follower instead of a Darlington stage). When point 43 is used instead of DMN2, a suitable intermediate voltage is used instead of the full swing VSS/VPP.

The circuit 40 operates as follows: when a control voltage $\overline{V_{in}}$ = 5 V (V_{SS} = 0 V) is applied to the input 41, the switching transistor MN1 is turned on and hence also the protection transistor MN2. The transistor MN2 (and the transistor MN3) is similar to the transistor shown in Fig. 1C and deviates therefrom in that use is made of p^- semiconductor material instead of n^- semiconductor material, *etc.* The voltage at the gate GMN3 decreases to approximately V_{SS}, so that the transistor MN3 is turned off. The voltage at the junction point 42 decreases to approximately $3V_{PP}/4$, governed by the resistance ratio:

$$\frac{R42 + R43}{R41 + R42 + R43}$$

The voltage at the junction point 43 decreases to approximately V_{PP} - 10 V, again governed by a resistance ratio:

$$\frac{R43}{R41 + R42 + R43}.$$

The bipolar transistor Q42 is turned on and the voltage at the junction point 45 will amount to V_{PP} - 10V + $|V_{BE}|$, V_{BE} being the base-emitter voltage of Q42. The transistors MP1 and MP2 are then turned on, like the transistors MP3 and MP4 whose gates GMP3 and GMP4 carry the same potential as the gate GMP2 because the transistor MN3 is turned off as described above. Because the transistors MP1-MP4 are turned on, the output O4 is connected to a voltage of approximately V_{PP}, depending on the load. It is important to ensure that no voltage differences of more than 10 V occur across the gates or across the drains and sources of MP1, MP2, MP3 and MP4. Therefore, no breakdowns are to be expected in this condition. The transistor Q41 is also turned off, because the emitter and the base BQ41 carry the same voltage. No current flows into the resistance chain R45, R46 and R47 from the output O4, because the transistor MP5 which is connected as a diode is polarized in the reverse direction. A load (in this case represented by a resistance RL and a capacitance CL) may be connected to the output O4. This load may be, for example a vacuum fluorescence display element which is powered *via* the transistors MP1-MP4.

When the control voltage at the input 41 is reset to 0 V, the transistor MN1 is turned off and the voltage at the gate GMN3 increases to V_{PP}. The transistor MN3 is turned on and a current will flow through the voltage divider R44-R48 and the "diode" MP5. The gate GMP1 of the transistor MP1 is connected to V_{PP}, so that the transistor MP1 is turned off. The transistor Q42 is turned off, because the voltage at the emitter, being connected to the point 45, is lower than the base voltage amounting to V_{PP}. The voltage divider R44-R48 is proportioned so that a voltage of < 10 V remains between the source and the drain of each of the transistors MP1, MP2, MP3 and MP4. As a result, in each transistor voltage stress is avoided. Breakdowns of sources and drains, in bulk, do not occur because each transistor is situated in its own n^- tub which is electrically connected to the relevant source.

The base of the transistor Q41 carries approximately V_{ss} = 0 V. The current through the resistance R48 produces a voltage increase between the base and emitter of the transistor Q41, which is thus turned on and pulls the output O4 to approximately V_{SS} + $|V_{BE}|$.

The invention is not restricted to the described embodiments. Further embodiments are readily feasible within the scope of the invention. For example, the parasitic transistors could be constructed so as to have polysilicon gates or aluminium gates.

Claims

1. A circuit which is integrated on a semiconductor substrate and which comprises a first and a second supply voltage terminal for application of a comparatively high voltage, an input and an output, there also being provided a switching transistor, a protection transistor and a sub-circuit, the switching transistor and the protection transistor being connected in series, the gate of the switching transistor being connected to the input, the source of the switching transistor being connected to a first power supply terminal, and the drain of the protection transistor supplying a signal for the sub-circuit during operation, an output of the sub-circuit being connected to the output and the gate of

the protection transistor receiving a fixed voltage, characterized in that the protection transistor is conceived so that it limits the voltage at the drain of the switching transistor.

2. An integrated circuit as claimed in Claim 1, characterized in that the gate of the protection transistor is provided on the field oxide layer of the integrated circuit.

3. An integrated circuit as claimed in Claim 1 or 2, characterized in that the switching transistor is provided with an extended drain.

4. An integrated circuit as claimed in Claim 1 or 3, characterized in that the protection transistor is provided with an extended drain and an extended or normal source.

5. An integrated circuit as claimed in any one of the Claims 1 to 4, characterized in that the gate of the protection transistor is connected to the second power supply terminal.

6. An integrated circuit as claimed in any one of the Claims 1 to 5, characterized in that the circuit comprises a third transistor which is connected in series between the switching transistor and the protection transistor, its gate being connected to a fixed voltage of a value between the gate voltage of the protection transistor and the first power supply voltage.

7. An integrated circuit as claimed in Claim 6, characterized in that the switching transistor, the protection transistor and the third transistor are p-channel MOS transistors, the p^+ drain terminal of the third transistor being situated in a p^- well which extends as far as the p-channel underneath the gate.

8. An integrated circuit as claimed in any one of the Claims 1 to 7, characterized in that the sub-circuit comprises a resistance.

9. An integrated circuit as claimed in any one of the Claims 1 to 8, characterized in that the sub-circuit comprises a current amplifier circuit.

10. An integrated circuit as claimed in Claim 9, characterized in that the current amplifier circuit is an emitter-follower circuit.

11. An integrated circuit as claimed in Claim 10, characterized in that the emitter-follower circuit comprises two vertical integrated bipolar transistors forming a Darlington pair.

12. An integrated circuit as claimed in Claim 10 or 11, characterized in that the drain terminal of the protection transistor is connected to the second supply voltage terminal *via* a series connection of at least two resistances, the base of a bipolar transistor being connected to the junction of the series connection and the drain terminal, the emitter being connected to the junction of a first and a second resistance of the series connection and to the output.

13. An integrated circuit as claimed in Claim 12, characterized in that the base of a second bipolar transistor is connected to the emitter of the first bipolar transistor, and that the emitter of the second transistor is connected to the junction of the second and a third resistance and constitutes the output of the circuit.

14. An integrated circuit as claimed in any one of the Claims 10,11,12 or 13, characterized in that the bipolar transistor or transistors is (are) formed in a respective p^- well in n^- semiconductor material, the base terminal being formed by a p^+ region and the emitter being formed by a n^+ region in the p^- well, the collector of the transistor being made of the n^- material.

15. An integrated circuit as claimed in any one of the Claims 12 or 13, characterized in that the resistances are formed as a p^- well in the n^- material.

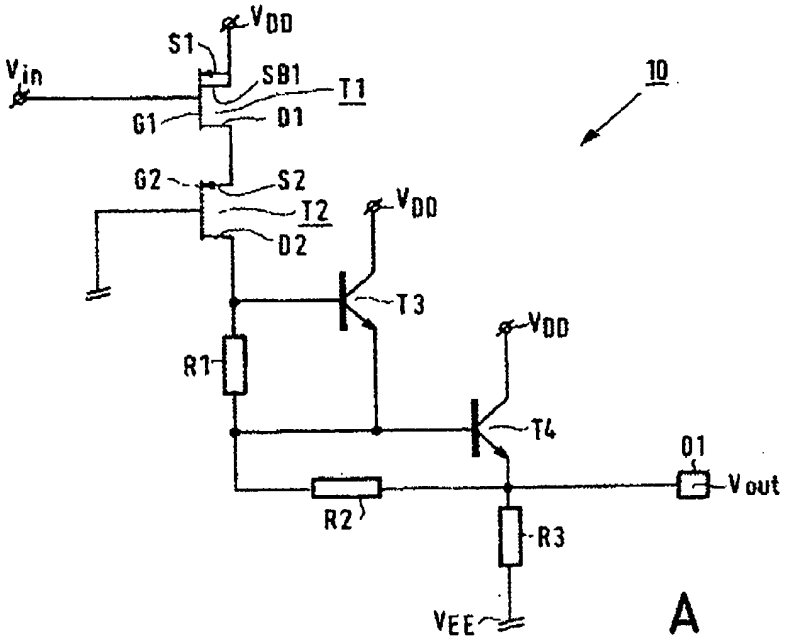
16. An integrated circuit as claimed in Claim 1, 3 or 4, characterized in that the drain and the source of the protection transistor are formed by p^- wells in n^- material, p^+ regions for contacting being formed in the p^- wells.

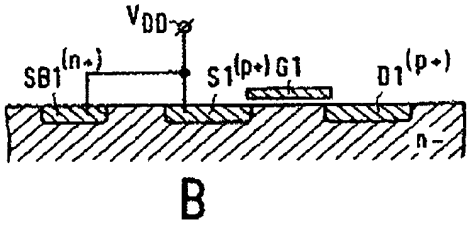
17. An integrated circuit as claimed in any one of the Claims 1 to 5, characterized in that the sub-circuit comprises a further switching transistor whose source is connected to the second supply voltage terminal, whose gate is connected to the drain of the protection transistor, and whose drain is connected to the first one of a series-connected cascode of further protection transistors, the drain of the last further protection transistor of the cascode being connected to the output, the gates of the cascode of further protection transistors being connected *via* a series connection of resistances, the output being connected to the emitter of a switch-off transistor whose collector is connected to the first supply voltage terminal and whose base is connected, *via* a resistance, to its emitter and to the drain of a

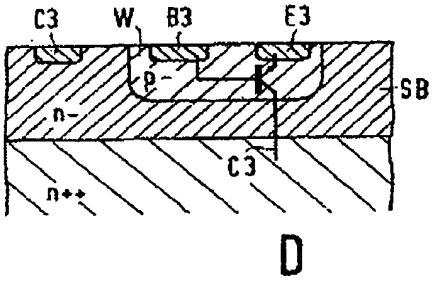
further transistor whose source is connected to the first supply voltage terminal and whose gate is connected to the drain of the protection transistor, the series connection of resistances being proportioned so that the voltages at the drain-gate junctions and at the drain-source junctions of the further switching transistor and the further protection transistors are limited.

18. A circuit integrated on a semiconductor substrate, comprising a first and a second supply voltage terminal, an input, and an output whereto a load to be driven by the circuit can be connected, a transistor and a sub-circuit being connected in series between one of the two supply voltage terminals and the output terminal, the gate of the transistor receiving a control signal, characterized in that the electrode of the transistor connected to the sub-circuit is either a p^+ or an n^+ region, formed in a p^- well or an n^- well, respectively, which is provided either in n^- or p^- material, respectively, and which extend as far as underneath the relevant gate.

19. An integrated circuit as claimed in Claim 18, in which a further transistor is connected in series between the sub-circuit and the transistor, its gate receiving a fixed voltage of a value which is between the voltages at the supply voltage terminals, characterized in that the drain as well as the source of the further transistor are either p or n regions which are formed by p^- or n^- wells, respectively which are provided either in n^- or in p^- material and which extend as far as underneath the gate of the further transistor.







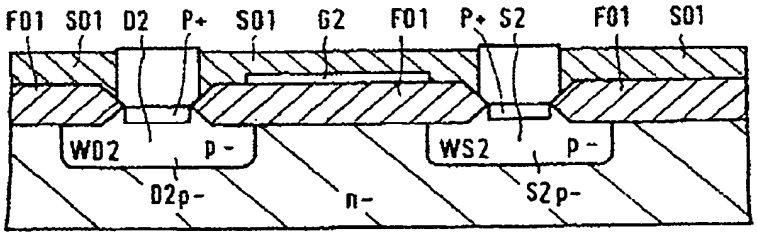
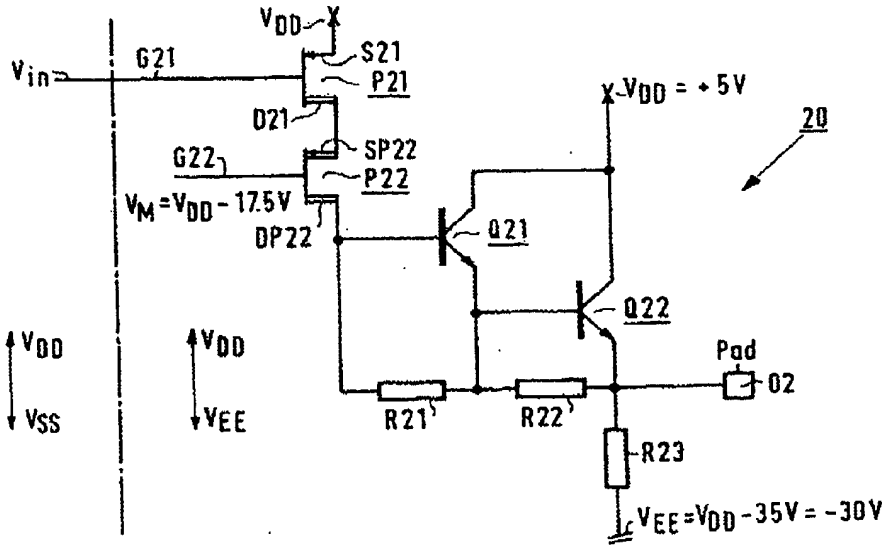
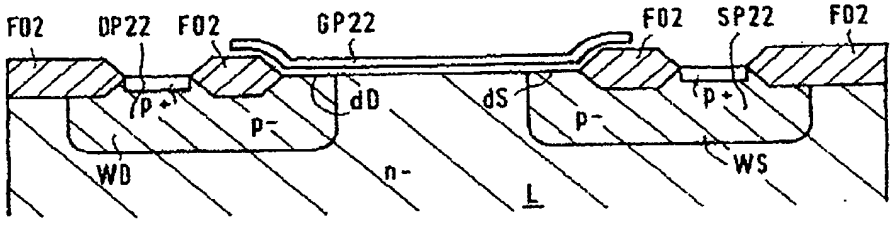


FIG.1



A



B

FIG.2

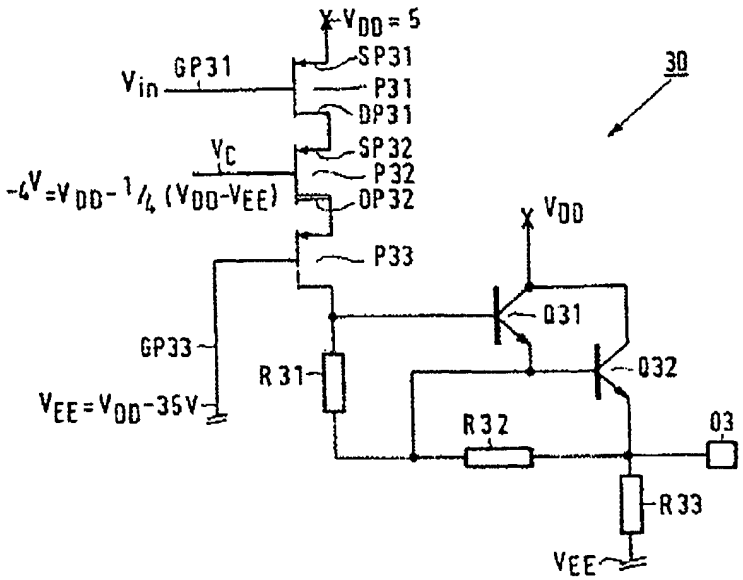


FIG.3

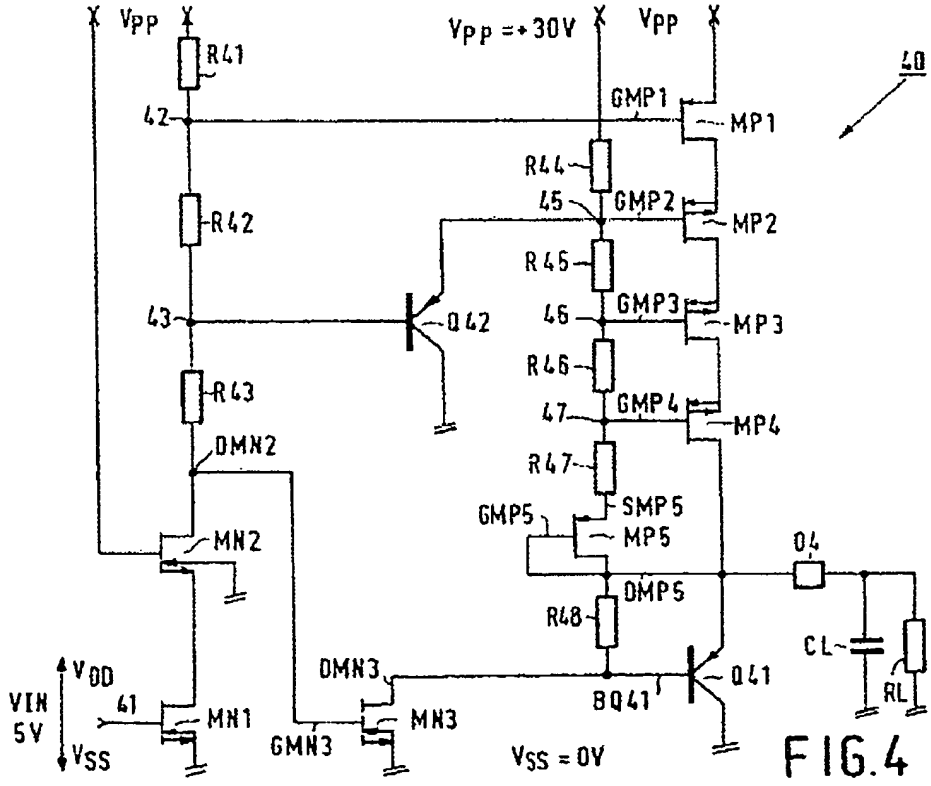


FIG.4

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(54) **Integrated semiconductor circuit including protection means.**

(57) The invention relates to a circuit which is integrated on a semiconductor substrate in order to drive a load, (for example, a VFD) by means of a comparatively high voltage (for example, 35 V), comprising a first and a second supply voltage terminal for application of the comparatively high voltage, an input, and a load output whereto a load to be driven by the circuit can be connected, there also being provided a switching transistor, a protection transistor and a sub-circuit, the switching transistor and the protection transistor being connected in series, the gate of the switching transistor being connected to the input, the source of the switching transistor being connected to a first supply voltage terminal, and the drain of the protection transistor supplying a signal for the sub-circuit during operation, the output of the sub-circuit being connected to the load output and the gate of the protection transistor receiving a fixed voltage, the protection transistor being conceived so that it limits the voltage at the drain of the switching transistor.

EP 0 561 451 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 20 0667

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
D,A	PROCEEDINGS OF THE IEEE 1987 CUSTOM INTEGRATED CIRCUITS CONFERENCE (CAT. NO.87CH2430-7), PORTLAND, OR, USA, 4-7 MAY 1987, 1987, NEW YORK, NY, USA, IEEE, USA, pages 267-267, MUHLEMANN K ET AL 'A 30 V row/column driver for flat-panel liquid crystal displays' ---	1-19	H01L27/02
A	EP-A-0 360 991 (SGS THOMSON MICROELECTRONICS) 4 April 1990 * abstract; figure 1 * ---	1-19	
A	EP-A-0 217 525 (ADVANCED MICRO DEVICES INC) 8 April 1987 * column 4, line 24 - line 27; figure 2 * -----	18,19	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 September 1995	Vendange, P

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